Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **Vcc**

**.051”**

**.051”**

**MASK**

**REF**

**2 1 14**

**13**

**12**

**11**

**10**

**6 7 8 9**

**3**

**4**

**5**

**HCT00T**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” min.**

**Backside Potential: Isolated**

**Mask Ref: HCT00T**

**APPROVED BY: DK DIE SIZE .051” X .051” DATE: 12/14/22**

**MFG: TEXAS INST / HARRIS THICKNESS .011” P/N: 54HCT00**

**DG 10.1.2**

#### Rev B, 7/19/02